(a) a first switching fabric having a configuration based on a first one of the implementation levels; and (b) a second switching fabric, coupled to the first switching fabric, having a configuration based on a second one of the implementation levels compatible with the first switching fabric.

In accordance with another broad system aspect of the present invention, a switch based upon a plurality of opto-electrical-physical implementation levels includes: (a) n first switching elements implemented by a recursive 2-stage construction technique, each of the first switching elements having m output ports and having a configuration based on a first one of the implementation levels; (b) m second switching elements implemented by a recursive 2-stage construction technique, each of the second switching elements having n input ports and having a configuration based on a second one of the implementation levels; and (c) an interface circuit interposed between the n first switching elements and the m second switching elements, wherein each of the first switching elements has a configuration based on a first one of the implementation levels compatible with the interface circuit and each of the second switching elements has a configuration based on a second one of the implementation levels also compatible with the interface circuit, the interface circuit having: mn input ports to cooperatively interconnect with the mn outputs of the n first switching elements; nm output ports to cooperatively interconnect with the nm inputs of the m second switching elements; and interconnections between the mn input ports and the mn output ports corresponding to a pre-determined exchange.

Moreover, the pre-determined exchange can correspond to an output exchange relative to the first switching elements, an input exchange relative to the second switching elements, or a combination of both.

In accordance with a broad method aspect of the present invention, a method for physically implementing a switch based upon a plurality of opto-electrical-physical implementation levels includes: (a) implementing n first switching elements, each of the first switching elements having m output ports and a switching fabric which either is a primitive switching circuitry or has a configuration based on a first one of the implementation levels; (b) implementing m second switching elements, coupled to the n first switching elements, each of the second switching elements having n input ports and a switching fabric which either is a primitive switching circuitry or has a configuration based on a second one of the implementation levels compatible with the first switching elements; and (c) configuring a 2-stage interconnection of the n first switching elements and m second switching elements by one of the implementation levels, wherein the implementation of the 2-stage interconnection is compatible with the first switching elements and the second switching elements.--.

A1 Cont.

Please replace lines 1-3 on page 13 as follows: --

FIG. 21B depicts a (1 2 3) permutation on an 8×8 exchange;

FIG. 21C depicts a (3 1) permutation on an 8×8 exchange;

A2

FIG. 21D depicts a combined (1 4)(2 3) permutation on an 8×8 exchange;--.

Page 215, replace line 5 as follows: "cell" with --cells--.

Page 218, replace line 9 as follows: --surface 7407 of a rectangular interface board, and the output switching elements are--.

Page 219, replace line 2 as follows: --realization of a "fiber-array package". Each I/O switching element in a fiber-array--.

Page 220, add after line 1: --Once a PCB is resulted from a step of PCB implementation, it cannot be used in another step of PCB implementation, and the same for the IC chip.--.

Page 221, replace line 9 as follows: --construction and is not implemented in any of the aforementioned levels. Such a--.

Page 223, replace line 14 as follows: --interconnection network associated with the sub-tree rooted at the internal node 20071. The--.

Please replace page 230, namely, the "Abstract of the Disclosure", with the following:

--ABSTRACT OF THE DISCLOSURE

Physical implementation of the switching fabric of a massive broadband switching network constructed from recursive 2-stage interconnection. The recursive 2-stage construction is realized through a hierarchical levels of implementation, including inside-chip implementation, PCB implementation, orthogonal packaging, interface-board packaging and fiber-array packaging. Smaller switches resulted from lower levels can be employed as the switching elements in the construction of a larger switch at a higher level of implementation. Such a hierarchical levels of implementation provides great